



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	Docket No.:	2003-0449/24061.103
Yu Jen Chen, et al.	§		
	§		
Serial No.:	§	Examiner:	Siek, Vuthe
10/810,926	§		
	§		
Filed:	§	Art Unit:	2825
March 25, 2004	§		
	§		
For:	§	Conf. No.	1917
A Method and System for	§		
Alerting An Entity to Design	§		
Changes Impacting the	§		
Manufacture of a Semiconductor	§		
Device in a Virtual FAB	§		
Environment	§		

DECLARATION UNDER 37 C.F.R. §1.131

We, Yu Jen Chen and Jiann-Yeh Ou, being duly sworn, depose and say:

1. That we are the inventors for the above-identified Patent Application;
2. That we have reviewed the claims of this Application;
3. That we conceived in Taiwan (Republic of China), a member of the World Trade Organization, prior to June 30, 2003, the earliest effective date of the cited United States Pre-Grant Publication No. 2005/0125763, the invention as set forth in the above-captioned application, and in particular, a method of manufacturing a semiconductor device comprising generating, by a first entity, design information useable for designing semiconductor devices, supplying, by the first entity, design information to a second entity, designing, by the second entity, a semiconductor device using the design information, and alerting the second entity by the first entity if there is a change in the design information that would impact the manufacture of the semiconductor device.
4. Attached as Exhibited A is a copy of our "TSMC Invention Disclosure" that was prepared and provided to our employer prior to June 30, 2003 evidencing conception of the above-captioned invention.
5. That from before June 30, 2003 to March 25, 2004, the filing date of the above-captioned application, we diligently worked toward reducing the claimed invention to practice

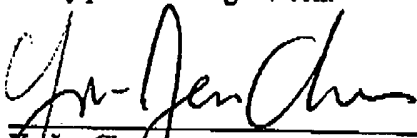
Serial No. 10/810,926  
Declaration under 37 C.F.R. §1.131

Docket No. 2003-0449/24061.103  
Customer No. 42717

and worked with patent counsel in the preparation of a patent application for the claimed invention. At no time did we abandon, suppress, or conceal the invention claimed in the above-captioned application.

That the statements made herein are of our own knowledge and are true and made on information and belief that are believed to be true.

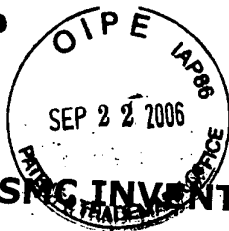
We acknowledge that any willful false statements and the like made herein are punishable by fine or imprisonment, or both, and may jeopardize the validity of the application or any patent issuing thereon.

  
Yu Jen Chen

Dated: Sept. 18, 2006

  
Jiann-Yeh Ou

Dated: Sep. 18, 2006



SECURITY B  
TSMC-RESTRICTED  
D.

**Status:** 待智財處處處理

Current Processor: 023437: 施冠妙

[illegible]

- Title of invention - (English only)  
A method of auto-finding & notifying inconsistency of building blocks & associated technology related substance of chip level during logic & physical design phase
- Related disclosure(s) -
- Assignee - 本發明屬於 1.TSMC 或 2.由TSMC與其他公司共同擁有  
● 1. TSMC ○ 2. TSMC &
- Laboratory Notebook / 研究紀錄簿相關資訊  
This idea was shown on page of the laboratory notebook with serial number of (such as 2002-00036).
- Please attach a copy of the related pages.
- Invention related information / 本發明相關資訊 -
1. Will this invention be disclosed, published, utilized, commercialized or implemented in Customer's product(s)?  
● No. ○ Yes. When (ex. 2003/04/24) 請務必填寫本發明之預定論文發表或展覽或販賣或實施於客戶產品的日期, 以加速申請流程.
2. Other special request :

● Classification –(Multiple choices are possible / 以下 1 至 4 項可多選)

1. Where will the invention be used / 本發明的潛在使用者：

- ☐ (Others)  
☒ At TSMC  
☐ Unknow  
☐ Probably will not be used  
☒ Used by most IC companies

2. Technology generation / 本發明適用於 (應用於一般技術請選擇 General, 0.25um 以上或 65nm 以下請選擇 others) :

- ☒ General ☐ 0.18um ☐ 0.13um ☐ 65nm ☐ Unknown  
☐ 0.25um ☐ 0.15um ☐ 90nm ☐ Others

3. Technology / 本發明應用在 (應用於一般技術請選擇 General, 無法歸類請選擇 others) :

- ☒ All Technology ☐ Image sensor ☐ Mixed-Signal/RF ☐ SiGe  
☐ DRAM ☐ Logic ☐ MRAM ☐ SRAM  
☐ Embedded ☐ MEMS ☐ NVM ☐ Others

4. Field of invention / 本發明的技術領域 (若無法歸類, 請選擇 Others) :

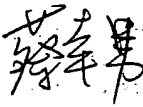

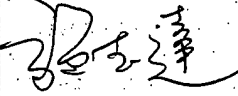

- |   |   |  |                                     |
|---|---|--|-------------------------------------|
| <input type="checkbox"/> Device                     | <input type="checkbox"/> Equipment/Litho/Mask     | <input type="checkbox"/> Module/Diffusion  | <input type="checkbox"/> Software   |
| <input checked="" type="checkbox"/> Business method | <input type="checkbox"/> Equipment/Thin Film      | <input type="checkbox"/> Module/Etch       | <input type="checkbox"/> Testing/Qf |
| <input type="checkbox"/> Circuit design             | <input type="checkbox"/> Integration              | <input type="checkbox"/> Module/Litho/Mask | <input type="checkbox"/> Others     |
| <input type="checkbox"/> Equipment/CMP              | <input type="checkbox"/> Manufacturing Technology | <input type="checkbox"/> Module/Thin Film  |                                     |
| <input type="checkbox"/> Equipment/Diffusion        | <input type="checkbox"/> Module/CMP               | <input type="checkbox"/> Package/Assembly  |                                     |

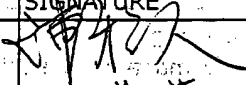


- References similar to the invention / 與本發明相關的論文及/或專利 - (Please search for related patents on USPTO website / www.uspto.gov)
  1. keyword(s) used / 專利查詢所使用的關鍵字 : inconsistency detect, discrepancy detect
  2. Related patent number(s) / 相關的專利號碼 :
  3. Related Non-Patent article(s) and/or product(s) / 其他相關的論文名稱或產品型號 :
- Old method(s) or product(s) for performing the purpose of this invention / 目前方法簡介 (English only)  
prepare a check list and then manually & periodically search the related information to check by few persons
- Problems or disadvantages faced by old method(s) or product(s) / 目前方法所面臨的問題及缺點 (English only)
  1. too big efforts to check (to customer)
  2. accuracy depends on how often to start the check (to customer)
  3. no way to know more information about application of customer's design (to TSMC)
  4. few revision messages not tied to a specific customer product or design and to get clear attention (to TSMC)
  5. could not effectively help TSMC to get related evidence to manager library/IP vendors reaction
- General purpose of this invention / 發明目的 (English only) -
  1. provide customer-centric service to the product level
  2. proactive notification if inconsistency detected
  3. via design profiles (without violating customer privacy) collected, more application oriented knowledge could be built in TSMC
  4. leverage customer force to manage library/IP vendors to have their product compliant to the latest technology
  5. a pragmatic scheme to build the link between foundry - library/Ip vendor - customer - design
- Advantages of this invention / 本發明的好處或優點 (English only)
  1. proactive to check what impact on designs as soon as a documentation available
  2. automatic notification
  3. entry & maintaining efforts from VIP customers (not by TSMC)
  4. experience sharing for technology promotion and junior or less experience TSMC staffs (FAE, CAE, R&D) also could be educated by profiles
  5. profiles could be expanded as sort of KM to application domain
  6. give the major & early proceedings' message prior to changes made and avoid the surprise of last minute change
  7. library/IP vendors are also be pushed to update by explicit customers' usage
  8. evidence of library/IP adopted by customers to manage vendors
- Points of this invention thought to be novel, list by items. Please identify which elements/steps are must and which elements/steps are optional / 請逐項列舉為達成發明目的所使用的新方法或手段, 即, 本發明與目前方法的主要不同處, 並請指出必要及非必要元件 (English only)
  1. a design profile created for customer (must, scope of find&check)
  2. a pool to store building blocks (must, preset the schema)
  3. a pool to store technology related stuffs -- documentation (must, preset the schema)
  4. implementation WIP of chip (must, preset the schema)
  5. rule-based intelligent auto-finder to figure out the inconsistency (must, to find the inconsistent parts)
  6. a mechanism to share information (must)
  7. a notification subsystem (must)
  8. early warning scheme (must)
- Detailed description of this invention / 發明的詳細敘述, 至少需包括一最好的實施例, 及/或其他適用於本發明的範例 (English only)  
refer to attachment

- Other embodiments/methods/apparatus can be used to achieve the purpose of your invention by a potential infringer./其他可實施本發明目的的手段?或其他可迴避本發明的範例及做法? manually approach



- Attachments / 圖形請用附加檔 : patent AFN on customer design profile [REDACTED].ppt

	SIGNATURE OF WITNESS	DATE	SIGNATURE OF WITNESS	DATE
WITNESS: THE TWO WITNESSES WHOSE SIGNATURES APPEAR BELOW HAVE READ AND UNDERSTOOD THIS ENTIRE INVENTION DISCLOSURE.				

DISCLOSURE SUBMITTED BY			
INVENTORS' EMPNO	INVENTORS' NAME	INVENTOR'S SIGNATURE	DATE
008922	陳於人		
019696	歐建業		

Processing Log :



[REDACTED] -0449

[REDACTED]

# **A method of auto-finding & notifying inconsistency of building blocks & associated technology related substance of chip level during logic & physical design phase via a design profile**

YJ Chen & JY Ou

Design  
Service

Enabling Innovation

1



## **Advantages**

- provide customer-centric service to the product level
- proactive to check what impact on designs as soon as a documentation available
- automatic notification
- experience sharing for technology promotion and junior or less experience TSMC staffs (FAE, CAE, R&D) also could be educated by profiles
- profiles could be expanded as sort of KM to application domain
- give the major & early proceedings' message prior to changes made and avoid the surprise of last minute change
- library/IP vendors are also be pushed to update by explicit customers' usage
- evidence of library/IP adopted by customers to manage vendors

Design  
Service

Enabling Innovation

2



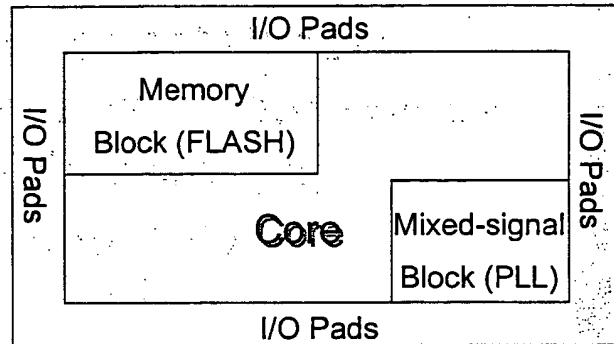
## Model of chip design -- view of building blocks & technical stuffs

### Building blocks (example)

IO Pad, PLL, embFLASH,  
core logic cell, etc

### Technology related substance (example)

DRM/DRC for blocks & chip level  
Layer definition for blocks & chip level  
Spice/LVS for blocks & chip level  
Definition of device formation  
RC extraction  
etc



*IC design is to integrate those components on the chip level.*

*Those must be derived from exactly consistent technology related substance  
and then the integrated chip must be verified by the same substance*

Enabling Innovation

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## Background -- current barriers to logic & physical design due to inefficiently get the up-to-day info

- Today a design needs about 4 ~ 12 months to tape out from logic implementation done.
- At different stage, designer need various foundry documentations such DRC/DRC, SPICE/LVS, etc (so called technology related stuffs) and some building blocks (library or IP) either from in-house or external vendors
- Those building blocks also are built upon the foundry documentations and those blocks usually have to implemented prior to product chip making
- It is very troublesome & dangerous if something changed. The related building blocks and chip both needed to re-spin the work fully or partially to compliant to the new
- Usually, designers got the foundry specific documents through their internal foundry manager or passive doc acquisition channels. The changes are not obvious to them, only get piece by piece, know at the last minute.

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# Solution – proactive manage consonance

– example : Design Rule → building blocks → full chip

know what foundry technology related substance used in a specific design

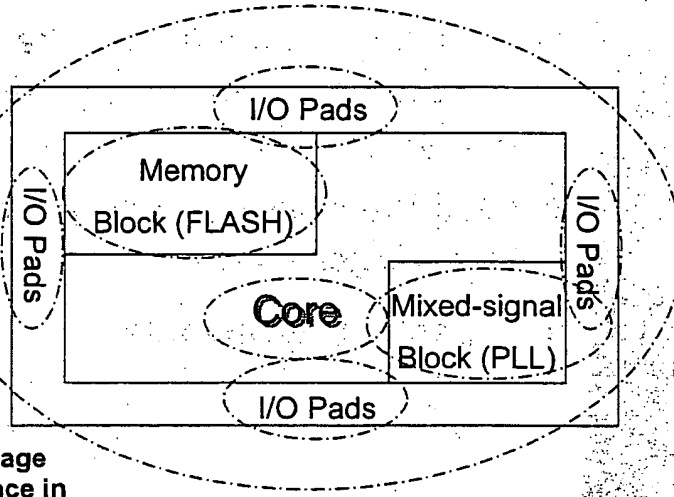
Know what building blocks & associated technology related substance used

Notify if inconsistency found

- Technology related substance
- Building blocks

Proactive give the major & early proceedings' message prior to changes made by foundry

⇒ via design profile to manage tape-out required consonance in a design



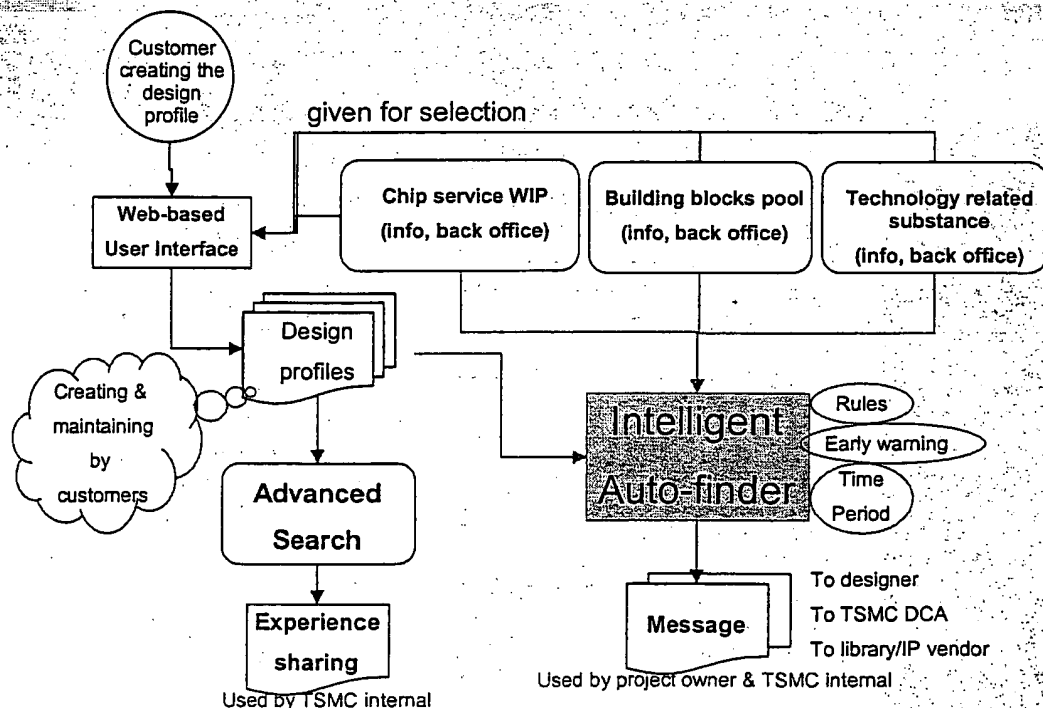
Means to be checked by one Design Rule

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5

Design Service

# Scheme diagram



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## Key features of auto-finder

- Rule-based find & check
- Building blocks & associated technology related substance on the chip level configurable via a design profile
- Give the major & early proceedings' message prior to changes made
- Proactive Notification

Design  
Service

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## Template to build the design profile

tsmc Design Service - Microsoft Internet Explorer

**DSD** Technology File Library Product Reference Flow FAQ Home  
Customer Request Customer Support Download Internal WebApp

CIS Portal Library Portal My Customer's Project Customer Profile Login ID: jchene

**My Customer's Project**

**Edit My Customer's Project**

Project ID:  selection

Company Name:

Project Name:

Project Leader:

Appication:

Memor Project Member:

Target Date:  Turn on tracking period

Technology File

DocID:  DocName:  Version:  DocType:  Add New Document

Library:  Add Library

Chip Implementation:  Add Chip Implementation

Project Name:

Save

8



## Select technology-specific tech file

Technology File - Microsoft Internet Explorer

Search Condition:  
Process: 013  
Document Type: ☐ DRC ☒ Keyword: calibre

Selection:  
Newest Document List  
T-013-ED-DR-001-C1 0.1a TSMC 0.13UM EMBEDDED DRAM 3P8M SALICIDE 1.0V3.3V & 1.2V3.3V  
T-013-ET-DR-001-C1 0.1a TSMC 0.13UM PLANAR TYPE EMBITRAM 1P8M SALICIDE 1.0V2.5V(A)  
T-013-LO-DR-001-C1 1.5T TSMC 0.13UM LOGIC 1P8M SALICIDE 1.0V2.5V, 1.2V2.5V, 1.0V3.3V, 1.2V3.3V  
T-013-LO-DR-004-C1 0.1b TSMC 0.13UM LOGIC 1P8M SALICIDE 1.0V1.2V CORE & 3.3V I/O (HS)  
T-013-LO-DR-005-C1 1.0t TSMC 0.13UM LOGIC 1P8M SALICIDE 1.5V2.5V(LP) DRC(CALIBRE)  
T-013-LO-DR-008-C1 0.1b TSMC 0.13UM LOGIC 1P8M SALICIDE 1.0V2.5V, 1.2V2.5V, 1.0V3.3V, 1.2V3.3V  
T-013-LO-DR-010-C1 1.0b TSMC 0.13UM HS+ LOGIC 1P8M SALICIDE 1.0V3.3V & 1.2V3.3V DRC

Selection outcomes or inputs:  
T-013-LO-DR-005-C1 1.0t  
TSMC 0.13UM LOGIC 1P8M SALICIDE 1.5V2.5V(LP) DRC(CALIBRE)  
COMMAND FILE (LOW POWER)

2 → Add Add & close

Status:  
• Tech. Changed  
• IP Tag in  
• Lib Product Doc  
• Contact us  
• Feedback

Process: 013  
Technology File  
Doc Name: DRC013-LO-DR-005-C1 Version: 1.0t Doc Type: TSMC 0.13UM LOGIC 1P8M SALICIDE 1.5V2.5V(LP) DRC  
Library: Add Library List  
Name: Version: Feature: Memo: delete  
Chip Implementation: Add Chip Implementation Case To List  
Product Name: Memo: Save

1

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## Select building blocks

LibraryIP - Microsoft Internet Explorer

Search Condition:  
Process: 013  
☒ At TSMC-Online ☐ 3rd vendor  
Technology: CL0130  
Category: PLL Keyword:

Selection:  
Library List  
pg13a1p2\_120b (Formal Release)  
pg13a1p3\_150a (Formal Release)  
pg13a1p3\_020115\_120a (Control Release)  
pg13a2p2\_150a (Formal Release)  
pg13a2p3\_150b (Formal Release)  
pg13a3p\_150c (Formal Release)

Selection outcomes or inputs:  
Name: pg13a1p3 Version: 150a  
Clock generator PLL, Fout 250MHz~1.0GHz

2 → Submit submit & close

Status:  
• Tech. Changed  
• IP Tag in  
• Lib Product Doc  
• Contact us  
• Feedback

Process: 013  
Technology File  
Doc Name: DRC013-LO-DR-005-C1 Version: 1.0t Doc Type: TSMC 0.13UM LOGIC 1P8M SALICIDE 1.5V2.5V(LP) DRC  
Library: Add Library List  
Name: Version: Feature: Memo: delete  
pg13a1p3 150a Clock generator PLL, delete  
Chip Implementation: Add Chip Implementation Case To List  
Product Name: Memo: Save

1

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## List of customer's project (example)

**Confidential-Security C**

© TSMC Design Service - Microsoft Internet Explorer

Home Library Product Reference Flow FAQ Contact Us

**DSD**

Technology File Library Product Reference Flow FAQ Contact Us

Customer Request Customer Support DTS Web 1000 Printmail Web App

CIS Portal Library Portal My Customer's Project Customer Profile Login ID: ychiena

# Library Product

- New release in 1 month
- Distribution
- Online Compiler
- Usage Statistic
- RCCB/SCCB
- Document
- Spice Schedule
- Tracking System
- Query
- Product
- Testchip Handling Status - Daily Status
- Tech. Changed
- IP Tag in
- Lib Product Doc
- Contact us (Feedback)

## My Customer's Project

### My Customer's Project

#### New Configuration

Advanced Search

Company	Project	Owner	Start	End
AE20 ADM TECHNOLOGY INC.	ADM2024	AE20	05/10/2002	05/15/2002
AS18 INGENUITY INC.	AS1812	AS18	07/15/2002	08/10/2002
CE207	CE207	CE207	12/17/2003	04/15/2004
C247 AMLOGIC, INC.	C24714	C247	10/10/2002	12/31/2002
U425 DSD SYSTEMS, INC.	U425	U425	05/15/2002	12/15/2002
U562 Gensys-Microchip	U562	U562	09/03/2002	11/30/2002
U768 Protecon Technology	U768	U768	11/05/2002	02/05/2003



## Contents of design profile (example)

**Confidential-Security C**

**DSD**

Technology File   Library Product   Reference Flow   FAQ   Home  
Customer Request   Customer Support   TSMC Gallery   Internal   Web App

CIS Portal   Library Portal   My Customer's Project   Customer Profile   Login ID-yicheng

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### Library Product

- New release in 1 month
- Distribution
- Online Compiler
- Usage Statistic
- RCCB/SCCB
  - Document
  - Spice Schedule
  - Timing System
- Query
- Product
  - Testchip Handling Status - Daily Status
  - Tech. Changed
  - IP Tag in
  - Lib Product Desc
  - Contact us
  - Feedback

---

### My Customers

Project Base Info

Company Name	A320 ADM TECHNOLOGY INC.
Project Name	ADM8629A
Process	025
Project Leader	
Application	WLAN SOC(1T) Access Point including MAC and PHY
Memo (Project Member)	
Target Date	06/10/2002 ~ 06/05/2002
Entity	研華 研華
Information Category	Yes

Chip Implementation Detail CIS Project

Chip Internal Technology File

ID#	File No.	Year	Doc Title	Status	Sign	Printed Date
LVS	1-025-LD-SH-005-CI	2.3a [target]	TSMC 0.25UM LDGIG1P5M SALICDF 2.3V/3.3V DRC (CAUBRE) COMMAND FILE	N/A		06/21/2002
DRC	1-025-LD-DR-OUT-CI	2.3a [target]	TSMC 0.25UM LDGIG1P5M SALICDF 2.3V/3.3V DRC (CAUBRE) COMMAND FILE	Online Effective		05/27/2002
DR	1-025-LD-DR-001	2.3a	TSMC 0.25UM LDGIG1P5M SALICDF 2.3V/3.3V DESIGN RULE	Online Effective		
DF	1-000-LD-DR-001	2.2 [target]	TSMC 0.25UM PADDESIGN RULE	100% Effective		

---

### Library

Name	Version	Release Date	Signed	Printed Date	Fast Download
lib27262 [DRC Version is not same 2.3a/2.3b]	250a [target]	05/23/2001	N/A	Finished	NO
lib27262 [DRC Version is not same 2.3a/2.3b]	252a	11/14/2002	N/A	Online Ready	NO
lib27262 [DRC Version is not same 2.3a/2.3b]	230a	10/02/2001	01/28/2002	Online Ready	YES

---

Chip Implementation

Project Name	ADM8629A	Model	S908
ADMSID	SHIMULIT	Design WIP	

Copy to a new Configuration   Email to someone   Print to ASCII file



## Outcome of auto-finder (example)

Confidential-Security C

TSMC Design Service - Microsoft Internet Explorer

**DSD** Technology File Library Product Reference Flow FAQ Home  
Customer Request Customer Support TSMC 9080 Internal Web App

CIS Portal Library Portal My Customer's Project Customer Profile Login ID:yichenn

Library Product

- New release in 1 month
- Distribution
- Online Compiler
- Usage Statistic
- RCCB/SCCB
- Document
- Spice Schedule
- Tracking System
- Query
- Product
- Testchip Handling Status - Daily Status
- Tech. Changed
- IP Tag In
- Lib Product Doc
- Contact us
- Feedback

Project Basic Info

Category Name: A370 ADM TECHNOLOGY INC.  
Project Name: ADM9C29A  
Process: 0.25  
Project Leader: [blank]  
Application: WLAN 802.11b Access Point including MAC and PHY  
Memo (Project Members): [blank]  
Target Date: 05/18/2002 - 08/15/2002  
Created: 1999-04-09  
Information Integrity: Yes

Chip-level technology file

DOC Type	DOC NO.	Version	ADDC Type	File	Order Effective	Order Effective Date
LVS	T-025-C0-SP-005-C1	2.04 (target)	TSMC 0.25UM LOGIC 1PSM SALICIDE	25V2 5W/13V LVS (CALIBRE) COMMAND FILE	N/A	05/21/2002
DRC	T-025-L0-DR-001-C1	2.36 (target)	TSMC 0.25UM LOGIC 1PSM SALICIDE	25V2 3V-DRE (CALIBRE) COMMAND FILE	N/A	05/21/2002
DR	T-025-U0-DR-001	2.3	TSMC 0.25UM LOGIC 1PSM SALICIDE	25V2 3V DESIGN RULE	Order Effective	
DR	T-000-L0-DR-00	2.2 (target)	TSMC AL BOND PAD DESIGN RULE		Order Effective	

Library

Name	Version	Process Date	Expired Date	Status	Checked Date	Is Download
002720x DRC Version 2.36 (2.30)	2504 (target)	05/23/2001	N/A	Expired	NO	
002720x DRC Version 2.36 (2.30)	2504 (target)	01/04/2002	N/A	Order Ready	NO	
002720x DRC Version 2.36 (2.30)	2304	10/02/2001	01/28/2002	Order Ready	YES	05/10/2002 LVS/DR

Chip Implementation

Project Name	File	Library	Memo	Flag
ADM9C29A	Simulation			Design File

Copy to new Configuration | EMail to Someone | Print to ASCII file

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## Search for experience sharing

Confidential-Security C

TSMC Design Service - Microsoft Internet Explorer

**DSD** Technology File Library Product Reference Flow FAQ Home  
Customer Request Customer Support TSMC 9080 Internal Web App

CIS Portal Library Portal My Customer's Project Customer Profile Login ID:yichenn

Library Product

- New release in 1 month
- Distribution
- Online Compiler
- Usage Statistic
- RCCB/SCCB
- Document
- Spice Schedule
- Tracking System
- Query
- Product
- Testchip Handling Status - Daily Status
- Tech. Changed
- IP Tag In
- Lib Product Doc
- Contact us
- Feedback

My Customers

My Customers Advance Search

Category: [blank]  
Project Name: [blank]  
Application: 802.11  
Memo (Project Members): [blank]  
Target Date: [blank]  
Document No.: [blank]  
Library Name: [blank]

Search [blank] Reset [blank]

14



# Experience found for reference (example)

Confidential-Security C

TSMC Design Service - Microsoft Internet Explorer

**DSD** Technology File Library Product Reference Flow FAQ Home  
Customer Request Customer Support Us RD 9000 Internal Web Apps

CIS Portal Library Portal My Customer's Project Customer Profile Login ID: yicheng

**Library Product**

- New release in 1 month
- Distribution
- Online Compiler Usage Statistic
- RCCB/SCCB
  - Document
  - Splice Schedule
  - Tracking System
- Query
- Product
- Testchip Handling Status - Daily Status
- Tech. Changes
- IP Tag in
- Lib Product Doc
- Contact us (Feedback)

**Search Result**

#	Company	Project Name	Process	Members	Application
1	Impiconn, Inc.	Jupiter2	018		WLAN 802.11b Baseband+MAC
2	ADM TECHNOLOGY INC.	ADM8628A	025		WLAN 802.11b Access Point including MAC and PHY
3	Impiconn, Inc.	Venus	018		WLAN 802.11g Baseband+MAC

Search Condition: Application= "802.11"

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